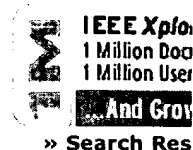


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- ☐ Standards

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- ☐ Journals & Magazines
- ☐ Conference Proceedings
- ☐ Standards

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- ☐ By Author
- ☐ Basic
- ☐ Advanced

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Design Automation Standards Committee of the IEEE Computer Society, USA;  
*This paper appears in: IEEE Std 1364-1995*

Publication Date: 14 Oct 1996

On page(s): -

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Number of Pages: x+666

INSPEC Accession Number: 5937860

**Abstract:**

The Verilog Hardware Description Language (HDL) is defined. Verilog HDL is a formal notation intended for use in all phases of the creation of electronic systems. Because it is both machine readable and human readable, it supports the development, verification, synthesis, and testing of hardware designs; the communication of hardware design data; and the maintenance, modification, and procurement of hardware. The primary audiences for this standard are the implementors of tools supporting the language and advanced users of the language

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